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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/721,310 | 11/25/2003 | Go Iwasaki | 81788.0261 | 7084 |

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| EXAMINER | |
|---|---|
| LE, THONG QUOC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/721,310 | IWASAKI, GO | |
| | Examiner | Art Unit | |
| | Thong Q. Le | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-19* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-19 are presented for examination.

### *Information Disclosure Statement*

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 11/25/2003.

3. Information disclosed and list on PTO 1449 was considered.

### *Specification*

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Objections*

5. Regarding claims 3-10, 12, 14, line 1, should be changed "A circuit" to – The output buffer circuit—.

6. Regarding claims 16-19, line 1, should be changed "A memory" to – The semiconductor memory—

The name of element in dependent claim should be used the same name as defined in independent claim.

7. Regarding claim 1, examiner does not find any drawing to show "a third input signal (IN3) are connected in series between said common node (C11) and a low-potential power supply (VSSQ)" as claim 1 discloses.

8. Regarding claims 11-12, applicant does not disclose any "first transistor", but applicant used "second transistors". Claim should be amended because when the name of element is a number, the number should be used in order. For example, the transistors have to be named "a first transistors"; then next can be named transistors being "a second transistors". It is avoided to make claimed invention confused and claim more clarity.

9. Regarding claims 13-14, as described above, claims used "third resistors' but "a first resistors" and "a second resistors" did not introduced in claim. Claim should be amended for more clearly.

### *Claim Rejections - 35 USC § 102*

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

11. Claims 1-4,7-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al. (U.S. Patent No. 6,366,114).

Regarding claim 1, Liu et al disclose an output buffer circuit (Figure 1) comprising: a plurality of unit circuits (Figure 1) in each of which a pull-up transistor (MOS2) controlled by a first input signal (173) is connected between a high-potential power supply (130) and common node (136) , and a first pull-down transistor (MOS1) controlled by a second input signal (175) and a second pull-down transistor controlled by a third input signal are connected in series between said common node and a low-potential power supply (132) ; an output terminal (125) connected to a common connecting point of said common nodes of said plurality of unit circuits; and first resistors (R3) formed respectively between said common nodes of said plurality of unit circuit and said common connecting point.

Regarding claim 2, Liu et al disclose an output buffer circuit comprising: a plurality of unit circuits in each of which a plurality of pull-up transistors (MOS2) controlled by an input signal (173) are connected in series between a high-potential power supply and common node (136) , and a plurality pull-down transistors (MOS1) controlled by an input signal (175) are connected in series between said common node and a low-potential power supply (132); an output terminal (125) connected to a common connecting point of said common nodes of said plurality of unit circuits; and

first resistors (R3) formed respectively between said common nodes of said plurality of unit circuits and said common connecting point.

Regarding claim 3-4, Liu et al. further comprising second resistors (R2) formed respectively between said high-potential power supply (130) and pull-up transistor (MOS2) and between said pull-down transistor (MOS1) and low-potential power supply (132) in each of said plurality of unit circuits, and a plurality of second resistors (R2) formed respectively between said high-potential power supply (130) and pull-up transistor (MOS2) and between said pull-down transistor (MOS1) and low-potential power supply (132) have the same resistance.

Regarding claims 7-10, Liu et al disclose the plurality of first resistors formed between the common nodes and output terminal have the same resistance (Figure 1 R3), and each of pull-up and pull-down transistor is MIS transistor (Figure 1), and the plurality of pull-up transistors have the same gate length and the same gate width and the plurality of pull-down transistors have the same gate length and the same gate (Figure 1).

Regarding claims 11-14, Liu et al. disclose an output buffer circuit (Figure1) comprising:

a plurality of unit circuits in each of which a pull-up transistor (MOS2) controlled by a first input signal(173) is connected between a high-potential power supply (130) and common node (136), and a pull-down transistor (MOS1) controlled by a second input signal (175) is connected between said common node and a low-potential power supply (132);

an output terminal (125) connected to a common connecting point of said common nodes of said plurality of unit circuits; and second resistors (R2) formed respectively between said high-potential power supply and pull-up transistor and between said pull-down transistor and low-potential power supply (R1) in each or said unit circuits, and wherein said plurality of second resistors formed respectively between said high-potential power supply and pull-up transistor and between said pull-down transistor and low-potential power supply have the same resistance (Figure 1).

12. Claim 15-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Curatolo et al. (U.S. Patent No. 6,737,886).

Regarding claims 15-19, Curatolo et al. disclose a semiconductor memory (Figure 1) comprising: a plurality of memory cells (Column 1, lines 15-21); a plurality of terminals including an output terminal (Figure 1, OUT) ; and an output buffer circuit (Figure 1) positioned adjacent to said memory cell, said output buffer circuit comprising a plurality of unit circuits in each or which a pull-up transistor (P1) controlled by a first input signal (P1cnt) is connected between a high-potential power supply (VDD) and common node (OUT_PAD) and a pull-down transistor (N1) controlled by a second input signal (N1cnt) is connected between said common node and a low-potential power supply (GND) , and comprising first resistors (Rout) connected respectively between said common nodes (OUT_PAD) of said plurality of unit circuits and a common connecting point of said common nodes (Figure 1), wherein the first resistors are formed between the output buffer circuit (Figure 1, OUT_PAD) and output terminal (Figure 1, OUT).

***Allowable Subject Matter***

13. Claims 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5-6 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Liu et al (U.S. Patent No. 6,366,114), Curatolo et al. (U.S. Patent No. 6,737,886), and others, does not teach the claimed invention having third resistors formed respectively between the pull-up transistors and common node and between the common node and pull-down transistors in each of the plurality of unit circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER